COMPLETE SET OF PENDING CLAIMS

What is claimed is:

1. (Currently Amended) A chip-scale package comprising:

a substrate having a first surface and an opposite second surface, the substrate composed of a controlled thermal expansion material;

a memory die having a first surface and an opposite second surface, the first surface of the memory die mounted facing the first surface of the substrate, the memory die is electrically coupled to the substrate using a plurality of rigid underside coupling members, the substrate having a coefficient of expansion that matches a coefficient of expansion of the memory die to within six parts per million per degree Celsius or less, wherein the second surface of the memory die remains completely exposed;

a plurality of solder balls mounted on the first surface of the substrate in a ball grid array configuration adjacent to the memory die, at least one of the solder balls electrically coupled to at least one of the underside coupling members;

a plurality of pads coupled to the second surface of the substrate, each pad electrically coupled to one or more of the plurality of solder balls ~~in a staggered routing scheme~~; and

one or more electronic components mounted on the second surface of the substrate in an area ~~substantially~~ opposite of the memory die, wherein the combined distance that an electronic component and the memory die protrude from the substrate is less than the distance that a solder ball and pad protrude from the substrate.

2. (Previously Amended) The chip-scale package of claim 1 further comprising:

electrically conductive traces on the first surface to electrically couple at least one solder ball to the memory die directly.

3. (Previously Amended) The chip-scale package of claim 1 wherein the plurality of rigid underside coupling members are a second plurality of solder balls.

4. (Previously Amended) The chip-scale package of claim 1 wherein five sides of the memory die are completely exposed and the first surface of the memory device is substantially exposed for improved heat dissipation.

5. (Currently Amended) A chip-scale package comprising:

a substrate having a first surface and an opposite second surface;

a semiconductor device mounted on the first surface of the substrate using a plurality of electrical conductors, the semiconductor device having a first surface and an opposite second surface, the first surface of the semiconductor device mounted facing the first surface of the substrate, wherein the second surface of the memory ~~die~~ device remains completely exposed for improved ventilation;

a plurality of solder balls mounted on the first surface of the substrate in a ball grid array configuration adjacent to the semiconductor device, at least one of the solder balls electrically coupled to the semiconductor device; and

a plurality of pads coupled to the second surface of the substrate, each pad electrically coupled to one or more of the plurality of solder balls ~~in a staggered routing scheme~~ which, when a plurality of chip-scale packages ~~is~~ are stacked together, causes a solder ball of a first chip-scale package to be uniquely electrically coupled with an electrical conductor of a semiconductor device mounted on a second chip-scale package N levels from the first chip-scale package, where N is an integer greater than two.

6. (Previously Amended) The chip-scale package of claim 5 further comprising:

one or more electrical components mounted on the second surface of the substrate in an area substantially opposite of the semiconductor device.

7. (Cancelled)

8. (Previously Amended) The chip-scale package of claim 6 wherein the combined distance that one or more electrical components and the semiconductor device protrude from the substrate is less than the distance that a solder ball and pad protrude from the substrate.

9. (Currently Amended) The chip-scale package of claim 5 wherein the substrate includes a controlled thermal expansion material with a coefficient of expansion that ~~substantially~~ matches the coefficient of expansion of the semiconductor device to within six parts per million per degree Celsius or less.

10. (Cancelled)

11. (Previously Amended) The chip-scale package of claim 5 further comprising:

electrically conductive traces on the first surface to directly couple at least one solder ball to the semiconductor device.

12. (Original) The chip-scale package of claim 5 wherein the semiconductor device is a silicon memory device.

13.-14. (Cancelled)

15. (Currently Amended) A stackable electronic assembly comprising:

a plurality of chip-scale packages, the plurality of chip-scale packages arranged in a stacked configuration, each chip-scale package including

a substrate having a first surface and an opposite second surface, the substrate composed of a controlled thermal expansion material;

a semiconductor device coupled to traces on the first surface of the substrate using underside coupling members;

a plurality of solder balls mounted on the first surface of the substrate ~~in a ball grid array configuration adjacent to the semiconductor device~~, at least one of the solder balls electrically coupled to the semiconductor device; and

a plurality of pads coupled to the second surface of the substrate, each pad electrically coupled to one or more of the plurality of solder balls ~~in a staggered routing scheme~~,

~~wherein all chip-scale packages in the stacked configuration have identical routing traces~~

the substrate having a coefficient of expansion that matches a coefficient of expansion of the semiconductor device to within six parts per million per degree Celsius or less.

16.-19. (Cancelled)

20. (Currently Amended) A memory module comprising:

a main substrate with an interface to couple the memory module to other devices; and

one or more stacks of memory devices coupled to a first surface of the main substrate,

at least one stack of memory devices including

a plurality of chip-scale packages, the plurality of chip-scale packages arranged in a stack, ~~all chip-scale packages in the stack having identical routing traces at every level of the stack,~~ each chip-scale package including

a substrate having a first surface and an opposite second surface,

a memory semiconductor die electrically coupled to traces on the first surface of the substrate, ~~and~~

~~a plurality of solder balls mounted on the first surface of the substrate adjacent to the memory semiconductor die, at least one of the solder balls electrically coupled to the memory semiconductor die~~

wherein the substrate is composed of a controlled thermal expansion material,

the substrate has a coefficient of expansion that matches a coefficient of expansion of the memory semiconductor die to within six parts per million per degree Celsius or less.

21. (Currently Amended) The memory module of claim 20 wherein

~~the substrate is composed of a controlled thermal expansion material,~~

~~the substrate has a coefficient of expansion that substantially matches a coefficient of expansion of the memory semiconductor die to within six parts per million per degree Celsius or less,~~

~~wherein~~ five sides of the memory semiconductor die are completely exposed and a sixth side of the memory semiconductor die is ~~substantially~~ exposed for improved heat dissipation~~, and~~

~~each chip-scale package further includes~~

~~a plurality of pads coupled to the second surface of the substrate, each pad electrically coupled to one or more of the plurality of solder balls in a stepped staggered routing scheme, and~~

~~one or more electronic components mounted on the second surface of the substrate in an area substantially opposite of the memory semiconductor die, wherein the combined distance that an electronic component and the memory semiconductor die protrude from the substrate is less than the distance that a solder ball and pad protrude from the substrate~~.

22. (Cancelled)

23. (Original) The memory module of claim 20 wherein the memory module is a dual inline memory module.

24. (Original) The memory module of claim 20 further comprising:

one or more stacks of memory devices coupled to a second surface of the main substrate.

25.– 27. (Cancelled)

28. (Currently Amended) The stackable electronic assembly of claim 15, the semiconductor device having a first surface and an opposite second surface, the first surface of the semiconductor device mounted towards the first surface of the substrate, wherein the second surface of the ~~memory die~~ semiconductor device remains completely exposed for improved ventilation.

29. (Currently Amended) The stackable electronic assembly of claim 28 wherein five sides of the semiconductor device are completely exposed and the first surface of the memory device is ~~substantially~~ exposed for improved heat dissipation.

30. (Currently Amended) The stackable electronic assembly of claim 15 further comprising:

one or more electrical components mounted on the second surface of the substrate in an area ~~substantially~~ opposite of the semiconductor device, wherein the combined distance that an electronic component and the semiconductor device protrude from the substrate is less than the distance that a solder ball and pad protrude from the substrate.

31.-32. (Cancelled)

33. (New) The chip-scale package of claim 5 wherein first surfaces of the semiconductor device is partially exposed for heat dissipation.

34. (New) The chip-scale package of claim 33 wherein the remaining four surfaces of the memory semiconductor device are completely exposed for heat dissipation.

35. (New) A chip-scale package comprising:

a substrate having a first surface and an opposite second surface, the substrate composed of a controlled thermal expansion material; and

a semiconductor device having a first surface and an opposite second surface, the first surface of the memory device mounted facing the first surface of the substrate, the memory device is electrically coupled to the substrate, the substrate having a coefficient of expansion that matches a coefficient of expansion of the memory device to within six parts per million per degree Celsius or less, wherein the second surface of the memory device remains completely exposed.

36. (New) The chip-scale package of claim 35 wherein the first surface of the memory device remains partially exposed for improved heat dissipation, the remaining five surfaces of the memory semiconductor device completely exposed for heat dissipation.

37. (New) A chip-scale package comprising:

a substrate having a first surface and an opposite second surface;

a semiconductor device mounted on the first surface of the substrate using a plurality of electrical conductors, the semiconductor device having a first surface and an opposite second surface, the first surface of the semiconductor device mounted facing the first surface of the substrate, wherein the first surface of the memory device remains partially exposed for improved heat dissipation; and

a plurality of solder balls mounted on the first surface of the substrate in a ball grid array configuration adjacent to the semiconductor device, at least one of the solder balls electrically coupled to the semiconductor device.

38. (New) The chip-scale package of claim 37 wherein the second surface and remaining four surfaces of the memory semiconductor device are completely exposed for heat dissipation.

39. (New) A memory module comprising:

a main substrate with an interface to couple the memory module to other devices; and

a plurality of chip-scale packages arranged in one or more stacks, each stack coupled to the main substrate, each chip-scale package including

a substrate having a first surface and an opposite second surface,

a memory die having a first surface and an opposite second surface, the first surface of the memory die mounted facing the first surface of the substrate, wherein the first surface of the memory die remains partially exposed for improved heat dissipation, and

a plurality of solder balls mounted on the first surface of the substrate in a ball grid array configuration adjacent to the memory die, at least one of the solder balls electrically coupled to the semiconductor device.

40. (New) The memory module of claim 39 wherein the second surface and remaining four surfaces of the memory semiconductor device are completely exposed for heat dissipation.